

REMARKS

The above amendments to the above-captioned application along with the following remarks are being submitted as a full and complete response to the Official Action dated July 23, 2004. In view of the above amendments and the following remarks, the Examiner is respectfully requested to give due reconsideration to this application, to indicate the allowability of the claims, and to pass this case to issue.

Status of the Claims

Claims 1-7 and 19 are under consideration in this application. claims 8-18 are being cancelled without prejudice or disclaimer. Claims 1-7 are being amended, as set forth in the above marked-up presentation of the claim amendments, in order to more particularly define and distinctly claim applicants' invention. A new claim 19 is being added to recite other embodiments described in the specification.

Additional Amendments

The claims are being amended to correct formal errors and/or to better recite or describe the features of the present invention as claimed. All the amendments to the claims are supported by the specification.

Applicants hereby submit that no new matter is being introduced into the application through the submission of this response.

Formality Rejections

Claims 1-18 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite and incomplete for omitting essential structural cooperative relationships such as in the example of "said plurality of first wiring with said first pitch in relation to said plug". The Examiner contended that it is not clear as to how a single plug could be connected to the "first wiring" of a multiple sub-wiring structures.

The semiconductor memory device of the invention (e.g., Embodiment 4: pp. 14-18; Figs. 15, 22), as now recited in claim 1, comprises: a plurality of first wirings (701), each of which is located along a first direction (B-B) with a first wiring pitch (2F in Fig. 15); a plurality

of chalcogenide material layers (203 in Fig. 22), each of which is located along said first direction (B-B); a plurality of second wirings (803), each of which is connected with a corresponding one of said chalcogenide material layers (203), and is located over said corresponding one of said chalcogenide material layers (203) and along said first direction (B-B); and a plurality of vertical transistors, each of which is formed over said corresponding one of said first wirings (701) and under a corresponding one of said second wirings (803) and is comprised of a source region (504), a drain region (505), a channel region (603) sandwiched between said source region (504) and said drain region (505), a gate insulating film formed on all sides of said channel region (603) and a gate electrode (403) formed on said gate insulating film and surrounding said all sides of said channel region (603). The drain region (505) is electrically connected with said corresponding one of said second wirings (803) through corresponding one of said chalcogenide material layers (203). The source region (504) is electrically connected with said corresponding one of said first wirings (701). Gate electrodes (403) of two adjacent ones of said vertical transistors in a second direction (A-A), which intersects perpendicularly with said first direction (B-B), are connected with each other (Figs. 15, 17 & 22), and gate electrodes (403) of two adjacent ones of said vertical transistors in said first direction (B-B) are separated from each other (Figs. 14-15, 18).

The device (claim 2; Figs. 4-5) further comprises a plurality of plugs (10). The source region (504) is electrically connected with said corresponding one of said first wirings (701) through a corresponding one of said plugs (*"A cell wiring (701) and select transistor may be electrically connected by this plug later (p. 9, 2nd paragraph)."*).

The device (claim 7; Fig. 15) further comprises: a plurality of word lines (403 in Fig. 15), each of which extends along said second direction (A-A) with a word line pitch (3F) and is comprised of said gate electrodes (403) which are connected with each other in said second direction (A-A). The first wiring pitch (2F) is smaller than said word line pitch (3F).

As recited in the new claim 19 (Fig. 22), the gate electrode (403) is formed by a side wall surrounding said source region (504), said channel region (603) and said drain region (505).

As claims 1-2 and 7 are being amended to clarify the structural connections between the elements as requested by the Examiner, the withdrawal of the outstanding informality rejection is in order, and is therefore respectfully solicited.

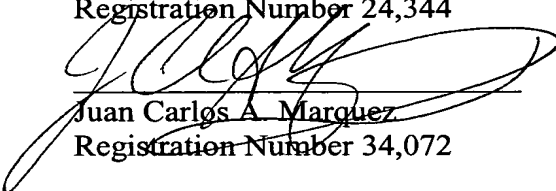
Conclusion

In view of all the above, clear and distinct differences as discussed exist between the present invention as now claimed and the prior art reference upon which the rejections in the Office Action rely, Applicant respectfully contends that the prior art references cannot anticipate the present invention or render the present invention obvious. Rather, the present invention as a whole is distinguishable, and thereby allowable over the prior art.

Favorable reconsideration of this application is respectfully solicited. Should there be any outstanding issues requiring discussion that would further the prosecution and allowance of the above-captioned application, the Examiner is invited to contact the Applicant's undersigned representative at the address and phone number indicated below.

Respectfully submitted,

Stanley P. Fisher
Registration Number 24,344



Juan Carlos A. Marquez
Registration Number 34,072

REED SMITH LLP
3110 Fairview Park Drive, Suite 1400
Falls Church, Virginia 22042
(703) 641-4200

January 21, 2005

SPF/JCM/JT